Amendments to the Drawings:

The attached sheet of drawings includes changes to Figures 5-6. This sheet, which includes Figs. 5-6, replaces the original sheets including Figs. 5-6.

Attachment: Replacement Sheet

REMARKS

This amendment is being filed along with a Request for Continued Examination (RCE) in response to the final Office Action having a mailing date of March 24, 2008. Various claims are amended as shown. New claim 25 is added. No new matter has been added. With this filing, claims 1-25 are pending in the application.

I. Supplemental information disclosure statement (IDS)

A supplemental IDS along with copies of the non-U.S.-patent references listed therein are being submitted herewith. Because this supplemental IDS and accompanying references are being filed along with the present RCE, an IDS fee and/or an IDS certification are not required and therefore are not being submitted herewith.

It is kindly requested that an Examiner-initialed copy of this supplemental IDS be provided along with the next communication, so as to confirm that the references listed therein have been entered into the record and considered.

II. Amendments to the drawings and the specification

The final Office Action objected to the drawings for not showing "the common clock signal" that was recited in previous claims 1, 8, 12-13, and 17 and the "common clock" recited in previous claim 22.

To address these objections, a (same) clock signal CK is shown in the replacement sheet of drawings filed herewith, having amended Figures 5-6. It is kindly requested that the enclosed amended Figures 5-6 replace the Figures 5-6 that are currently on file. Support for these drawing changes can be found on page 14, lines 9-10 and elsewhere in the present application.

In view of these amendments to Figures 5-6, it is respectfully submitted that the drawing objections have been overcome, and it is therefore requested that such objections be withdrawn.

The SUMMARY section of the specification is amended as shown to remove explicit references to the claim numbers. This amendment is being made to avoid any

discrepancy between the written description and the claims, in view of claim cancellations, claim additions, and/or other changes to the claims that may result in claim renumbering in the potential issued patent.

III. Rejections under 35 U.S.C. § 112, first paragraph

The final Office Action rejected claims 1-21 under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the written description requirement. Specifically, the final Office Action alleged that the "common clock signal" recited in claims 1, 8, 12-13, and 17 was not found in the original disclosure.

It is respectfully submitted that the "common clock signal" does indeed meet written description requirements. For example, page 3, lines 6-7 and page 14, lines 9-10 of the written description explain that each of the two finite state machines at the respective transmission and reception ends is supplied with the "same clock signal."

Nevertheless, to facilitate prosecution and to provide further compliance with 35 U.S.C. § 112, first paragraph, claims 1, 8, 12-13, and 17 are amended herein to recite a "same clock signal" (instead of a "common clock signal") so as to more precisely correspond to the language used in the written description. Claim 22 is also amended to clarify that each of the first and second finite state machines receives the same clock signal. In view of these amendments to claims 1, 8, 12-13, 17, and 22 it is kindly requested that the written description rejection with respect to these claims and their respective dependent claims be withdrawn.

Claim 23 was also rejected under 35 U.S.C. § 112, first paragraph by the final Office Action, which alleged that the limitation "a register to store sorting patterns" is not located in the original disclosure. This rejection is traversed herein—it is respectfully submitted that claim 23 does indeed meet written description requirements. For example, page 12, lines 13-16 of the present application describes the FIFO register 12 as being supplied with and accumulating sorting patterns. Furthermore, page 17, lines 10-13 of the present application describes the FIFO register 12 as "stores temporarily both the data supplied by the transmitter 11 and the sorting patterns associated thereto" (emphasis ours). In view of this written description

in the original disclosure, it is therefore kindly requested that the written description rejection of claim 23 be withdrawn.

IV. Discussion of the claims and cited references

The final Office Action rejected claims 1-24 under 35 U.S.C. § 103(a) as being unpatentable over Curran (U.S. Patent No. 5,572,736) in view of Szepesi (U.S. Patent No. 5,680,300). For the reasons set forth below, these rejections are respectfully traversed. It is kindly requested that the rejections be reconsidered and withdrawn.

A. Independent claim 1

Independent claim 1 as amended herein recites, *inter alia*, "transmitting on at least one line of the bus the datum in said transmission format, and transmitting on one additional line of the bus a synchronization signal having the selected sorting pattern." Support for these amendments can be found, for example, on page 12, lines 11-12; page 16, lines 4-7; page 3, lines 17-18; page 10, lines 26-29; page 12, lines 13-20; and elsewhere throughout the present application.

It is respectfully submitted that these various limitations recited in amended claim 1 are not met by the cited references, whether singly or in combination.

For example, page 6 of the final Office Action admitted that "Curran may not explicitly teach push-pull bus driver used for synchronization." To supply these missing synchronization teachings of Curran, the final Office Action alleged that the push-pull driver disclosed in Szepesi's column 6, lines 18-34 provide synchronization. It is respectfully submitted that Szepesi does not cure the deficiencies of Curran.

More particularly, assuming *hypothetically* and *arguendo* that Szepesi's push-pull driver does provide synchronization, Szepesi nevertheless does not disclose, teach, or suggest that a synchronization signal provided by his push-pull driver would be providing informational content (specifically, providing the selected sorting pattern as recited in claim 1). Rather, Szepesi's synchronization signal is used merely for clocking. Column 6, lines 18-34 of Szepesi is reproduced below (emphasis ours):

> "The synchronization block 22, under control of the phase 2 clock output θ_2, cuts off the drive to sw4 during the first phase θ_1 of the clock; during phase 2 (θ_2 low), the synchronization block 22 enables sw4 to be driven. That is, during the clock's second phase θ_2 an analog switch 40 provides an analog signal path, i.e., one which accommodates a continuously variable signal, from the output of the amplifier 36 to the push-pull stage 38. During this phase, the gate voltages to n-channel FETs 42 and 44 are low, consequently FETs 42 and 44 are 'OFF' and the output of the amplifier 36 is conducted through the analog switch 40 and drives the push-pull stage 38 which, in turn, modulates the gate voltage of sw4. During phase 1 θ_2 is high, therefore analog switch 40 is non-conducting and FETs 42 and 44 are 'ON', shutting off drive current to the push pull stage 38 and turning sw4 'OFF'."

From the above-quoted passage of Szepesi relied upon by the final Office Action, it is evident that Szepesi does not provide a synchronization signal that has informational content (namely, the selected sorting pattern)—he only provides clocking. Since neither Curran nor Szepesi meet the limitations of claim 1 that require "a synchronization signal having the selected sorting pattern", claim 1 is allowable.

Claim 1 is further allowable over the cited references, since neither of these references disclose, teach, or suggest providing the data on at least one line of the bus and the sorting pattern (via the synchronization signal) on an additional line of the bus. More particularly, Curran maps data words into n-bit "code words" using a "mapping code" and uses a "switching code" to identify the mapping code that was used. However, Curran "incorporates" or "appends" the switching code (which identifies the mapping code that was used) in the transmitted code word, rather than transmitting the switching code using an additional line as required in claim 1.

Curran explains the following in his column 2, lines 60-65 and in column 4, lines 43-49 (emphasis ours):

> "In accordance with another aspect of the invention, a switching code identifying the mapping code used in the mapping of the data word into the n-bit code word selected for transmission is incorporated in the transmitted code word and is used in the receiving circuit to map the received code word into the original data word, as that data word existed prior to transmission … a plurality of mapping codes are generated, each identified by the state of the switch bits. Each mapping code is applied to the new data word and in each case, selected bits of the data word are complemented and the switch bits are appended to the resultant word to form a code word."

Thus from the above-quoted passage of Curran, by "incorporating" or "appending" his switching code ("switch bits") in the transmitted code word, he inherently/explicitly cannot meet the limitations of claim 1 that require at least one line of the bus to transmit the datum and an additional line of the bus to transmit the selected sorting pattern (via the synchronization signal). Stated in another way, Curran's technique of incorporating his switching code into the transmitted code word means that these two things (switching code and code word) are transmitted together on the same line, rather than on separate/multiple lines as reflected in claim 1.

Thus, since neither Curran nor Szepesi meet the limitations of claim 1 that require "transmitting on at least one line of the bus the datum …, and transmitting on one additional line of the bus a synchronization signal having the selected sorting pattern," claim 1 is further allowable over these references.

Furthermore, Curran is substantially a reworking of a conventional technique known as "bus-inverter", which is a redundant encoding technique that associates the n-bit encoded information with a redundancy which is made up of s-bit switching bits and which specifies which lines are to be complemented at the reception end to recover the original information. Curran discloses a switching code that identifies the bus lines that are to be inverted, and is a string as long as the number of bus lines: when a bit in the i-th position is "1",

the corresponding bus line is to be complemented at the reception end to recover the information transmitted. A 16-line bus has thus a switching code of the type "0001001011010011". In comparison, one embodiment provided by the present applicant involves, instead, the swapping pattern being a bit sequence that indicates the bus lines that are to be multiplexed, and is M.log2(M) long, where M is the bus switch cluster depth. If N=4, then the swapping pattern is 8 bit long. For example, a valid swapping pattern (namely a pattern that allows the transmitted information to be validly recovered at the reception end) is 0-2-3-1 (00101101 in binary). Not all the swapping patterns may be valid. For example, 0-1-0-3 (00010011 in binary) may not allow the transmitted information to be validly recovered at the reception end.

Claim 1 as amended is still further allowable over the cited references in that there are two synchronizations provided in claim 1. First, there a first synchronization using the above-discussed synchronization signal that provides the selected sorting pattern. Second, there is a second synchronization involving synchronization of sorting patterns using a same clock signal: "a succession of said sorting patterns generated at a transmission end and a succession of sorting patterns generated at a reception end are synchronized with each using a same clock signal supplied to said transmission and reception ends."

It is respectfully submitted that the dual synchronization of claim 1 is not found in the cited references. For example, page 6 of the final Office Action admitted that Curran does not teach that his push-pull driver is used for synchronization. Szepesi, in comparison and explained above, only provides a single sychronization for clocking purposes. Neither of these two references provides the two synchronizations of claim 1.

For all of the above reasons, it is thus respectfully submitted that claim 1 is allowable.

B. Independent claims 8 and 12

Independent claims 8 and 12 are amended in a manner generally similar to claim 1, using varying language. Specifically, claim 8 as amended recites, *inter alia*, the features of the synchronization signal having the optimal sorting pattern, transmitting the datum on at least one line, and transmitting the optimal sorting pattern (via the synchronization signal) on one

additional line. Furthermore, claim 8 recites synchronization of sorting patterns using a same clock signal, thereby also providing claim 8 with two synchronizations (the synchronization signal having the optimal sorting pattern and the synchronization of the sorting patterns).

Claim 12 as amended also recites, *inter alia*, the features of the synchronization signal having the selected sorting pattern, transmitting the datum on at least one line, and transmitting the selected sorting pattern (via the synchronization signal) on one additional line. Furthermore, claim 12 recites synchronization of sorting patterns using a same clock signal, thereby also providing claim 12 with two synchronizations (the synchronization signal having the optimal sorting pattern and the synchronization of the sorting patterns).

As previously explained above, Curran and Szepesi (whether singly or in combination) do not meet these limitations.

Hence, claims 8 and 12 are allowable.

C. Independent claims 13, 17, and 22

Independent claims 13 and 17 are amended to recite, *inter alia* and using varying language, transmitting an identity signal in addition to at least one signal that transmits the data. Hence, it is clear in claims 13 and 17 that the identity signal is separately transmitted from the data signal. As previously explained above, Curran does not meet these limitations, since he appends/incorporates his switching code (switch bits) into his transmitted code word, thereby transmitting them together in one signal (rather than as two signals as required in claims 13 and 17).

Independent claim 22 as amended herein recites, *inter alia*, that the datum is transmitted on at least one line and the synchronization signal is transmitted on one additional line. Again, Curran does not meet these limitations since he appends/incorporates his switching code into his code word, thereby transmitting them together on the same line.

Claim 22 is also further allowable since two synchronizations are recited (synchronization signal and synchronization of the sorting patterns using a same clock signal). This dual synchronization is not provided by either of the cited references, which at most provide only a singular synchronization.

Accordingly, claims 13, 17, and 22 are allowable.

D. New dependent claim 25

New dependent claim 25 recites that "first internal states of said first and second finite state machines correspond to a most probable sorting pattern determined according to analysis of traffic on said bus." Support for these limitations can be found on page 16, lines 12-20 of the present application.

It is respectfully submitted that Curran does not meet these limitations. For example, Curran is completely silent with respect to any probabilistic determination of the "switching code" that he will use.

Hence, claim 25 is allowable.

E. Dependent claims 5, 7, 9, 11, 14, 16, 18, and 20

Dependent claims 5, 7, 9, 11, 14, 16, 18, and 20 are amended to clarify that the state machine(s) recited therein receive the same clock signal. Pages 27-28 (sections 7-8) of the final Office Action have alleged that Curran does indeed disclose finite state machines. However, nothing was specifically cited from Curran with respect to such state machines receiving the same clock signal.

Accordingly, it is respectfully submitted that claims 5, 7, 9, 11, 14, 16, 18, and 20 are allowable.

F. Other claim amendments

Various other amendments are made to the claims as shown to provide consistent antecedent basis, to more precisely recite the subject matter contained therein, to make the terminology with and between the claims consistent given the amendments to the independent claims, and/or to otherwise place such claims in better form.

V. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the attorney of record (Dennis M. de Guzman) has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. de Guzman at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are believed to be allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

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